# A 0.5 to 4 GHz True Logarithmic Amplifier Utilizing Monolithic GaAs MESFET Technology

MARK A. SMITH, MEMBER, IEEE

*Abstract*—**The design of the true logarithmic amplifier is reviewed, and the sensitivity of the circuit's performance to design or process errors is investigated. Following this is a description of a GaAs monolithic dual-gain amplifier stage which has been developed for 0.5 to 4 GHz true logarithmic amplifier applications. This bandwidth is significantly greater than that of previously reported true logarithmic amplifier stages. A cascade of six of these stages has resulted in a logarithmic amplifier with a 70 dB dynamic range.**

## I. Introduction

LOGARITHMIC amplifiers are useful for compressing the dynamic range of signals prior to detection, so that detectors with limited dynamic range may be used in receiving systems to measure widely varying input signal amplitudes. Many types of logarithmic amplifiers have been developed [1], [2], and the type which is used in any particular application is determined by the system requirements. One type of logarithmic amplifier which is commonly used in systems which must perform signal processing functions on the phase of the incident signal is termed the true logarithmic amplifier, introduced by Woroncow and Croney in 1966 [3]. In the case of the true logarithmic amplifier, the output is a carrier frequency signal with voltage amplitude directly proportional to the logarithm of the input power level.

Excellent results have been obtained by constructing dual-gain stages as monolithic silicon amplifiers using bipolar transistors [4]. Many companies are now producing true logarithmic amplifiers using these techniques, with typical bandwidths of a few hundred megahertz centered in the VHF or UHF frequency range.

## II. The True Logarithmic Amplifier

The true logarithmic amplifier is composed of a cascade of dual-gain stages, as shown in Fig. 1. Each stage contains two independent amplifiers which share a common input. One amplifier has high gain and a low limiting power level, and the other has unity gain and a high compression point. When the outputs of these two paths are combined, the result is an amplifier stage with an abrupt change in gain at some input power level. The stage has moderate gain (typically 10 dB) at low power levels, and gain approaching unity at higher power levels, as shown in Fig. 2. Referring again to Fig. 1, the case of 10 dB gain stages requires a voltage gain $A$ of 2.16 or 6.7 dB to be combined with the unity gain path. An amplifier comprising a cascade of these stages will possess an output versus input characteristic which is a piecewise-linear approximation to the desired logarithmic function.

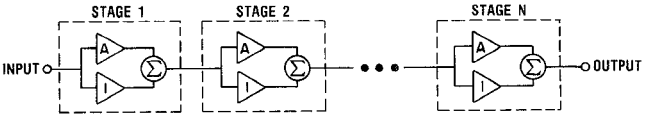



Fig. 1 Block diagram of a true logarithmic amplifier.

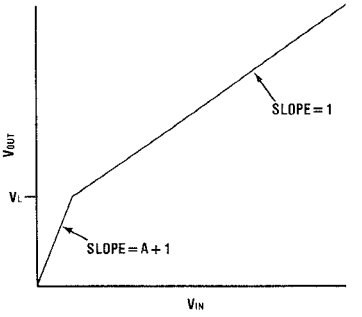



Fig. 2. Voltage gain characteristics of one dual-gain stage.

The characteristics of a true logarithmic amplifier consisting of six ideal dual-gain stages, each with 10 dB gain, are presented in Fig. 3. Barber and Brown [4] have shown that the breakpoints in the response lie on the line defined by

$$V_{\text{out}} = \left\{N + 1/A + \log_{(A+1)}[AV_{\text{in}}/V_L]\right\} V_L \quad (1)$$

where $V_L$ is the output limiting voltage of the limiting amplifier path, and $N$ is the total number of dual-gain stages. The maximum logarithmic error, or deviation of the approximating curve from a best fit straight line response, may be reduced by using more stages, each with less gain. For the case of 10 dB gain stages, the maximum error from a best fit line is about 0.8 dB. In practice, however, the transition of the dual-gain stages from their linear to limiting modes is somewhat gradual, an effect which reduces the sharpness of the breakpoints and makes them difficult to identify in the measured response of a true logarithmic amplifier utilizing 10 dB gain stages.

It is instructive to investigate the effects of stage gain and limiting power level errors on the characteristics of the true logarithmic amplifier. If, in the amplifier possessing the response shown in Fig. 3, gain $A$ is increased 10 percent from 2.16 to 2.38, the curve shown in Fig. 4

Manuscript received April 25, 1988, revised August 12, 1988
The author is with Armatek, Inc., Richardson, TX 75081.
IEEE Log Number 8824176.

0018-9480/88/1200-1986$01.00 ©1988 IEEE

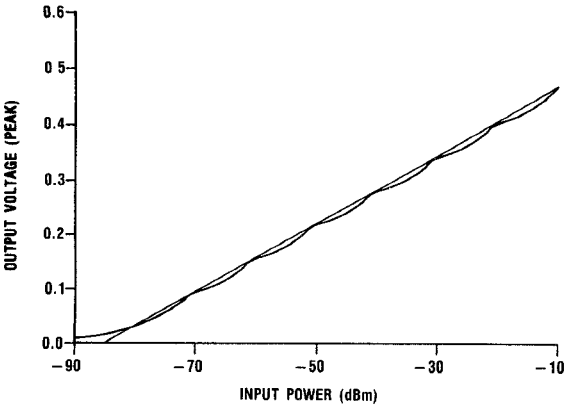



Fig. 3. Gain characteristics of a true logarithmic amplifier with 10 dB gain stages. The breakpoints of the approximating curve lie on the line defined by (1) in the text.

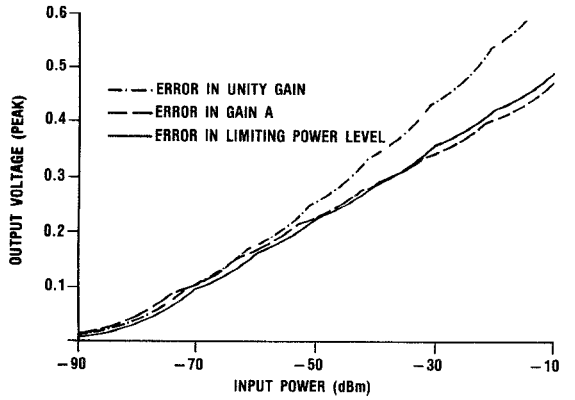



Fig. 4. Gain characteristics of a true logarithmic amplifier with stage gain and limiting power level errors.

results. The logarithmic slope of the amplifier has decreased from 6.3 to 6.0 mV/dB, but the linearity of the response has been retained. This is to be expected because changing the value of $A$ is exactly equivalent to changing the nominal gain of each stage. The effect of increasing the stage gain is to increase the dynamic range of the amplifier, at the expense of generating greater errors between the approximating and ideal logarithmic response curves. The maximum error from a best fit line has been increased in this case from 0.8 to 1.1 dB. Assuming that these errors do not become excessive, the fact that linearity is retained indicates that system errors induced by errors in the gain $A$ may be corrected after the logarithmic amplifier through the use of linear gain or attenuation.

Similarly, errors in the limiting power level of the higher gain path result in a response which retains linearity. As seen in Fig. 4, if the limiting power level of the higher gain path is increased 10 percent from $-8$ dBm to $-7.6$ dBm, the resulting logarithmic slope is changed from 6.3 to 6.6 mV/dB. Maximum error from a best fit line is not affected by errors in the limiting power level, as long as the limiting power level is sufficiently small relative to the compression point of the unity gain path.

These two previous cases are in sharp contrast to the case of error in the gain of the "unity gain" path. An amplifier composed of stages in which $A$ is 2.16 but the gain of the unity gain path is 10 percent in error will generate a nonlinear response curve (also shown in Fig. 4). This error cannot be corrected after the logarithmic amplifier except through the use of another nonlinear device. It is clear, then, that the most important constraint in the design of a true logarithmic amplifier is the accuracy of the gain of the unity gain path of each stage.

## III. Design

In this effort, the advantages of GaAs monolithic technology have been utilized to develop a monolithic dual-gain stage for the 0.5 to 4 GHz band. A schematic diagram of the circuit is shown in Fig. 5. A stage gain of 10 dB was chosen, but because a $-6$ dB resistive combiner was used rather than an ideal combiner, the gains of both amplifier paths were increased 6 dB relative to the ideal combiner case. The first path has 12.7 dB gain and a saturated output power of $-8$ dBm, and the second path has 6 dB gain and a saturated output power of $+11$ dBm.

A thin-film network external to the monolithic circuit contains the $-6$ dB resistive combiner in which the outputs of the two amplifier paths are combined to provide the linear gain of 10 dB at low power levels. Because of the low limiting power level in the higher gain path, the gain of the stage begins to decrease as input power exceeds $-20$ dBm. The stage gain asymptotically approaches 0 dB as input power is further increased. Additional circuit elements printed on the thin-film network are two shorted stubs which may be used for gain shaping and a series transmission line to equalize the insertion phase between the two paths.

With regard to insertion phase, it should be noted that, for proper operation of the true logarithmic amplifier stage, it is crucial that the outputs of the two gain paths be combined in phase. To allow broad-band operation, care was taken to ensure that an even number of inverting FET gain stages were used in each amplifier path. Because of this, the insertion phases of the two paths were easily equalized through the use of a series transmission line in the higher compression path, which contains fewer FET's. The predicted insertion phases of the two paths are shown in Fig. 6.

Fig. 7 is a photograph of the GaAs monolithic dual-gain amplifier. The circuit contains seven FET's, 29 GaAs resistors, and 18 capacitors for a total of 190 pF capacitance. The dimensions of the chip are 2.0 mm $\times$ 2.2 mm, and the thickness is 0.1 mm. Harmonic balance nonlinear analysis techniques were used to predict the compression point and the saturated output power of each amplifier path. This information was used in the selection of a 50 $\mu$m gate width FET for the output stage of the high-gain path and a 300 $\mu$m FET for the output stage of the lower gain path. All other FET's are of 150 $\mu$m gate width. A complete gain stage consisting of the amplifier chip and its associated thin-film network mounted on a carrier plate is seen in Fig. 8.

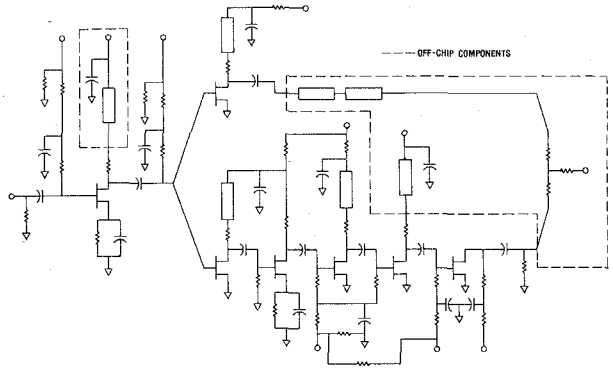



Fig. 5. Schematic diagram of one dual-gain stage.

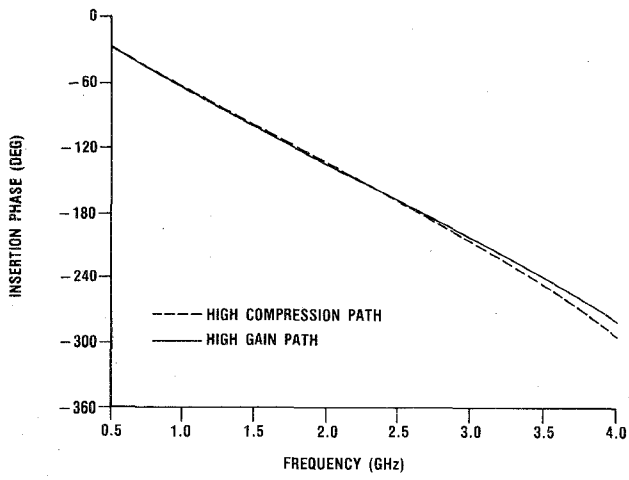



Fig. 6. Predicted insertion phases of the two paths.

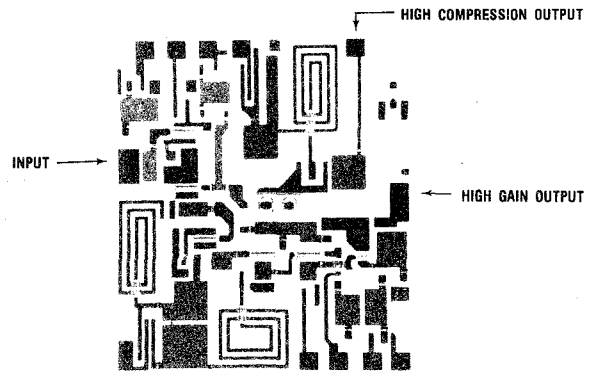



Fig. 7. Monolithic dual-gain amplifier chip.

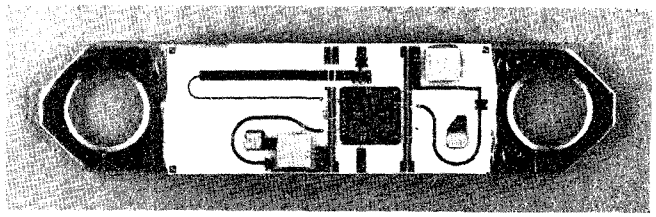


Fig. 8. Complete dual-gain stage.

## IV. Measured Performance

The gains of the two paths were individually evaluated using a test thin-film network which did not combine the outputs of the two paths. These gains are seen in Fig. 9.

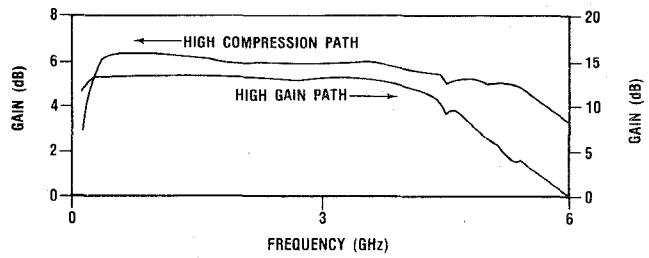



Fig. 9. Measured gain of the two paths of the dual-gain stage.

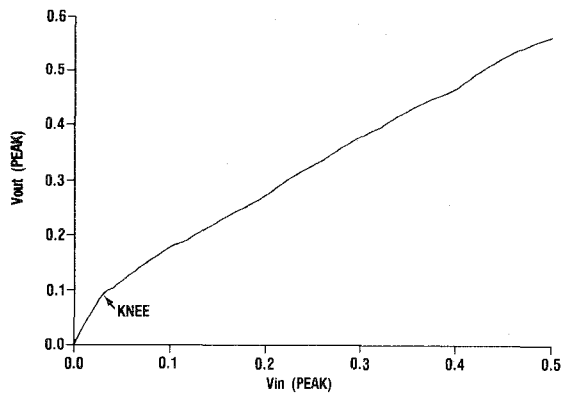



Fig. 10. Measured voltage gain characteristics of the dual-gain stage.

The higher gain path shows 12.7 ± 1 dB gain, and the gain of the high compression path is measured to be within 0.4 dB of its 6 dB target.

The measured voltage response of one dual-gain amplifier stage installed in the combining thin-film network is seen in Fig. 10. The axes are scaled in peak volts to show the knee in the gain response, which is characteristic of true logarithmic gain stages. Below the knee the slope is indicative of 10 dB linear gain, and above the knee the gain slope is unity until the lower gain amplifier eventually saturates. Fig. 11 shows the limiting process in the frequency domain, as the power gain of the dual-gain stage is shown for two input power levels. At a −30 dBm input power level, the stage gain is 10 ± 1 dB across the full 0.5 to 4 GHz frequency range. With an input power level of 0 dBm, the stage shows 1.6 ± 0.3 dB gain.

Fig. 12 is a picture of the six-stage logarithmic amplifier composed of these dual-gain amplifier stages. Regulation for dc voltages is included in the housing. Power requirements are +8 V at 0.6 A and −8 V at 50 mA. The overall response of the amplifier is seen in Fig. 13. At any given frequency in the 0.5 to 4 GHz band, the logarithmic error from a best fit line is less than ±3.5 dB across input power levels between −70 and 0 dBm. The fact that the curves do not lie on top of each other indicates an undesirable frequency dependence of circuit parameters. From the previous discussion of the effects of circuit errors on the logarithmic response, it is apparent that the unity gain paths have very accurate gain values, because each of the curves shows good linearity. However, in the case of the 1 GHz curve, the higher gain path exhibits both gain and limiting output power in excess of the design goals, resulting in greater output voltage for all

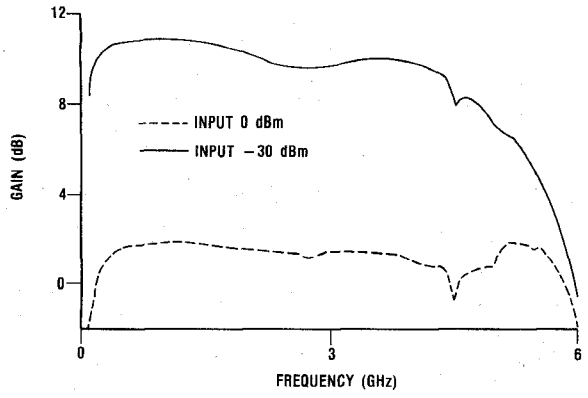



Fig. 11. Gain of the dual-gain stage at two input power levels.

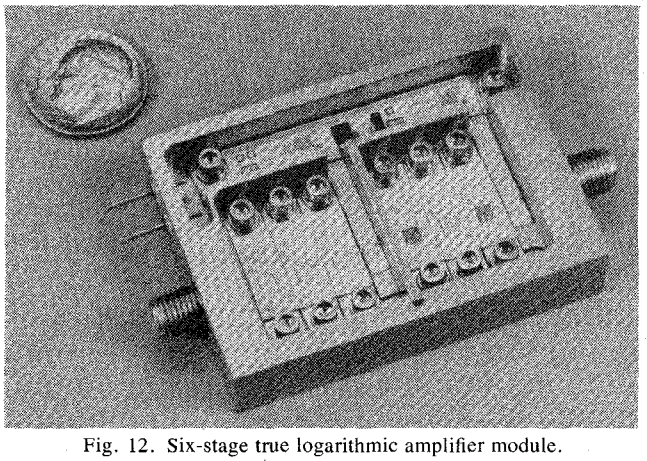


Fig. 12. Six-stage true logarithmic amplifier module.

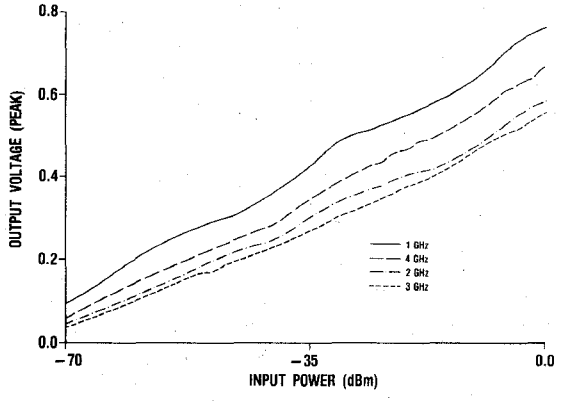



Fig. 13. Broad-band logarithmic amplifier response.

input power levels. These problems are presently being addressed in an effort to improve the amplifier's performance.

The amplifier was also characterized in the time domain. Fig. 14 shows the response of the amplifier to 15 ns pulses of a 500 MHz carrier. The top trace of the figure shows the pulse before attenuation to a −52 dBm level and injection into the logarithmic amplifier input. The resulting output pulse is seen in the bottom trace, lagging the input pulse by about 4 ns.

Because the limiting components in logarithmic amplifiers generate harmonics, it is desirable in many system applications to select a frequency band such that the harmonics of the input signal can never fall in band. If a band of 2 to 3 GHz is chosen and the lengths of the gain shaping stubs on the thin-film network are adjusted to yield the best amplifier performance within this band, the response of Fig. 15 results. In this case, less than ±5 dB error from a single best fit line is seen across frequency and powers between −70 and 0 dBm. Although it has not been experimentally verified, it is expected that the −6 dB resistive combiner used at the output of the dual-gain stage will supply sufficient isolation to make the stage tolerant of high reflection loads, both at fundamental and at harmonic frequencies. This will be important in the case where the logarithmic amplifier is followed directly by a bandpass filter which is highly reflective at harmonic frequencies.

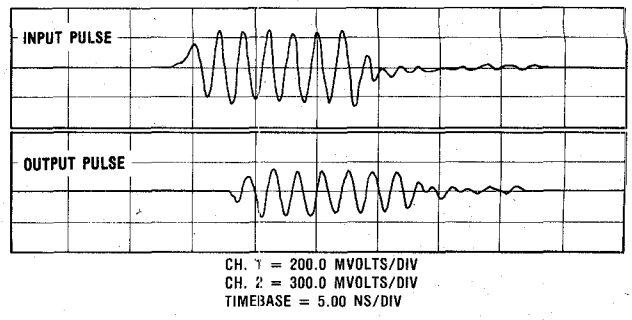



Fig. 14. Time-domain response of the logarithmic amplifier to 15 ns pulses of a 500 MHz carrier at −52 dBm level.

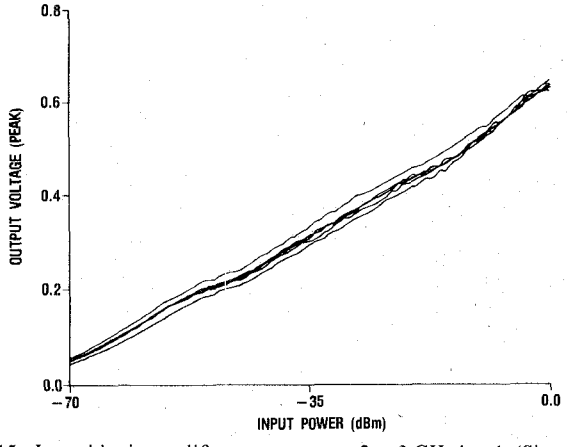



Fig. 15. Logarithmic amplifier response over 2 to 3 GHz band. (Six curves have been plotted, corresponding to 200 MHz steps.)

Insertion phase invariance as a function of input power level is another important performance parameter for a true logarithmic type amplifier. For the full bandwidth of 0.5 to 4 GHz, measured data indicate a maximum phase change of 14.5° for any 10 dB power increment in the −70 to 0 dBm range, and a 27° maximum error from the average insertion phase for any frequency and power level in these ranges.

## V. Conclusion

In conclusion, a monolithic GaAs dual-gain amplifier circuit has been developed, and a logarithmic amplifier utilizing a cascade of these devices has been designed,

built, and tested. The amplifier exhibits a 70 dB dynamic range and is operational over the 0.5 to 4 GHz band. This wide bandwidth will be useful in increasing the instantaneous information bandwidth of future microwave systems.

## Acknowledgment

The author is indebted to J. Vaillancourt for the hours he spent in the assembly and testing of the logarithmic amplifier modules. Additional thanks go to K. Anderson, T. Howard, J. Norris, and E. Reese for insightful and encouraging discussions.

## References

[1] R. S. Hughes, *Logarithmic Amplification*. Dedham, MA: Artech House, 1986.

[2] K. H. Lansdowne and D. E. Norton, "Log amplifiers solve dynamic-range and rapid-pulse-response problems," *Microwave Syst. News*, vol. 15, no. 11, pp. 99–109, Oct. 1985.

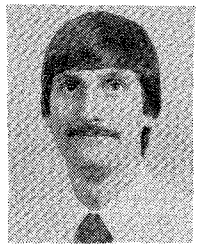
[3] A. Woroncow and J. Croney, "A true I.F. logarithmic amplifier using twin-gain stages," *Radio Electron. Eng.*, vol. 32, no. 3, pp. 149–155, Sept. 1966.

[4] W. Barber and E. Brown, "A true logarithmic amplifier for radar IF applications," *IEEE J. Solid-State Circuits*, vol. SC-15, pp. 291–295, June 1980.

[5] B. Loesch, "A UHF true logarithmic IF amplifier," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-9, pp. 660–664, Sept. 1973.

[6] E. Schmidt, "High-speed logamp surveys 2 to 6 GHz," *Microwaves & RF*, vol. 25, no. 7, pp. 135–136, July 1986.

*



**Mark A. Smith** (M'83) received the B.S. degree in engineering physics from the Colorado School of Mines in 1983 and the M.S.E.E. degree from Southern Methodist University in 1986.

He is presently responsible for microwave integrated circuit design and development as an Engineering Group Leader with Armatek, Inc., Richardson, TX. Mr. Smith was previously with the Microwave Laboratory of Texas Instruments, where he was involved in hybrid and monolithic microwave circuit design under several IR & D programs. Included in this work have been self-doubling oscillators, millimeter-wave mixers and couplers, and a complete millimeter-wave two-channel down-converter. Additionally, he has been responsible for the development of nonlinear device modeling algorithms for the optimization of FET power amplifier and mixer performance.

Mr. Smith is a member of Tau Beta Pi and Sigma Pi Sigma.